

# Jared Smolens

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## Education

**Carnegie Mellon University**, Pittsburgh, PA

Ph.D. in Electrical and Computer Engineering, Aug 2002 - Dec 2007

Recipient of the A. G. Jordan Award for academic excellence and exceptional service, May 2008

Research interests: Microarchitecture and multiprocessor architecture, performance, reliability

Thesis title: Fingerprinting: Hash-Based Error Detection in Microprocessors

Advisor: James C. Hoe

**Carnegie Mellon University**, Pittsburgh, PA

Master of Science in Electrical and Computer Engineering, Aug 2001 - May 2002

**Carnegie Mellon University**, Pittsburgh, PA

Bachelor of Science in Electrical and Computer Engineering

with University Honors, Aug 1997 - May 2001

## Selected Publications

- [1] **Detecting Emerging Wearout Faults**  
JC Smolens, BT Gold, JC Hoe, B Falsafi, and K Mai  
The Third IEEE Workshop On Silicon Errors in Logic - System Effects (SELSE-3), Apr 2007
- [2] **Reunion: Complexity-Effective Multicore Redundancy**  
JC Smolens, BT Gold, B Falsafi, and JC Hoe  
ACM/IEEE International Symposium on Microarchitecture (MICRO-39), Dec 2006
- [3] **TRUSS: A Reliable, Scalable Server Architecture**  
BT Gold, J Kim, JC Smolens, ES Chung, V Liaskovitis, E Nurvitadhi, B Falsafi, JC Hoe, and AG Nowatzky  
IEEE Micro Special Issue: Reliability-Aware Microarchitectures, Nov - Dec 2005
- [4] **Fingerprinting: Bounding Soft-Error Detection Latency and Bandwidth**  
JC Smolens, BT Gold, J Kim, B Falsafi, JC Hoe, and AG Nowatzky  
IEEE Micro, Top Picks from Computer Architecture Conferences, Nov - Dec 2004
- [5] **Efficient Resource Sharing in Concurrent Error Detecting Superscalar Microarchitectures**  
JC Smolens, J Kim, JC Hoe, and B Falsafi  
ACM/IEEE International Symposium on Microarchitecture (MICRO-37), Dec 2004
- [6] **Fingerprinting: Bounding Soft-Error Detection Latency and Bandwidth**  
JC Smolens, BT Gold, J Kim, B Falsafi, JC Hoe, and AG Nowatzky  
International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-11), Oct 2004

## Experience

**Oracle (was Sun Microsystems)**, Santa Clara, CA, Jan 2008 - present

Principal Software Engineer, Architecture Technology Group / Microelectronics

- Processor core performance and power modeling for SPARC T4 and future SPARC processors

**Carnegie Mellon University**, Department of ECE, Pittsburgh, PA  
Graduate Research Assistant, Aug, 2002 - Dec 2007

#### Major Research Activities

- **Reliable microarchitectures and systems**  
Developed a formal execution model for complexity-effective redundant execution and evaluated a chip multiprocessor-based implementation in simulation [2]; identified and isolated the primary performance factors in redundant multithreaded cores, proposed microarchitecture changes to recover performance [5]; proposed designs for reliable multiprocessor systems [3]
- **Hardware design**  
Demonstrated proof-of-concept fingerprint detection with fault injection in a commercial synthesizable Verilog CPU (Sun OpenSPARC) [1,4,6]
- **Performance modeling**  
Designed and implemented the CMP cache coherence protocol and switch-based network simulator for Flexus, an open-source timing simulator used by architects at Carnegie Mellon and outside institutions (<http://www.ece.cmu.edu/~simflex>)

#### Teaching

- 18-347, 18-447: Introduction to Computer Architecture (Fall 2003, Fall 2004)  
Lead TA, developed and supervised semester-long superscalar RTL processor project
- 18-545: Advanced Digital Design Project (Spring 2002)  
Project TA, supervised groups in a semester-long FPGA-based MP3 decoder design project
- 18-349: Introduction to Embedded Systems (Fall 2001)  
Project TA, supervised labs, performed grading

**Intel Corporation**, Santa Clara, CA, Summer 2005  
Graduate Intern, Test Technology Research Group

- Modeled and evaluated architectural fingerprints for soft error detection and manufacturing test applications on a full-chip IA-32 mobile core RTL model
- Investigated implementations of architectural fingerprints on IA-32 desktop and Itanium server core RTL models

**Unisys Corporation**, Malvern, PA, Summer 1999, Winter 1999 - Spring 2003  
Technical Intern, System Analysis Modeling and Measurement Group

- Responsible for writing, documenting and maintaining a multiprocessor cache simulator
- Performed collection and analysis of memory address traces for TPC-C workloads on mainframes for input to a detailed performance queuing model
- Performed initial architectural design, modeling and evaluation of coherence protocol optimizations for migratory sharing in commercial workloads

#### Skills

Languages: C, C++, Synthesizable Verilog, assembly (SPARC, x86), Java  
Software: Linux, Windows, Solaris, Virtutech Simics, Synopsys, user and kernel programming  
Hardware: P6-based microarchitectures, extensive knowledge of OpenSPARC T1  
Other Coursework: computer networks, optimizing compilers, databases

#### References

Available upon request.